AMENDMENTS

Please amend the above-referenced application as follows:

IN THE CLAIMS:

Please amend the claims as indicated below.

1. (Twice Amended.) An apparatus ~~for performing single-instruction multiple-data instructions using a single multiply-accumulate (MAC) unit~~, comprising:

a single multiply accumulate (MAC) unit configured to generate a data result responsive to a single-instruction multiple-data (SIMD) instruction, the data result having a first half and a second half;

a register communicatively coupled to the ~~multiply-accumulate~~ single MAC unit, the register configured to store the first half of the data result; and

a miscellaneous-logic unit configured to initiate the release of the first half of the data result from the register to synchronize the first half of the data result with the second half of the data result.

2. (Previously Amended.) The apparatus of claim 1, wherein said MAC unit generates the first half of the data result before the second half of the data result.

3. (Previously Amended.) The apparatus of claim 2, further comprising:

a register file configured to receive the first half of the data result substantially concurrently with the second half of the data result.

4. (Twice Amended.) The apparatus of claim 3, wherein said ~~miscellaneous-logic~~ (MAC) unit generates an exception result when said miscellaneous-logic unit determines the first half of the data result is erroneous.

5. (Twice Amended.) The apparatus of claim 4, wherein said miscellaneous-logic (MAC) unit is configured to initiate the release of one of the first half of the data result stored in said register or initiate the release of the exception result.

6. (Twice Amended.) A method for performing single-instruction multiple-data (SIMD) instructions using ~~a single multiply-accumulate unit~~, comprising the steps of:

providing a single multiply-accumulate (MAC) unit configured to generate a first half of a data result and a second half of a data result responsive to a single-instruction multiple-data (SIMD) instruction;

applying the first half of the data result at an input of a register;

using a miscellaneous-logic unit to generate an exception result; and

applying the first half of the data result and the second half of the data result at an input of a buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are valid, otherwise applying an exception result at the input of the buffer when the miscellaneous-logic unit determines that the first half of the data result and the second half of the data result are invalid.

7. (Previously Amended.) The method of claim 6, further comprising:

latching a first operand into said MAC unit; and

latching a second operand into said MAC unit.

8. (Previously Amended.) The method of claim 7, further comprising:

generating the first half of the data result from the first operand; and

generating the second half of the data result from the second operand.

9. (Previously Amended.) The method of claim 8, further comprising:

latching the first half of the data result in a miscellaneous logic unit; and

latching the second half of the data result in the miscellaneous logic unit.

10. (Previously Amended.) The method of claim 9, further comprising:

generating the exception result from the first half of the data result and the second half of the data result.

11. (Twice Amended.) An apparatus for performing single-instruction multiple-data (SIMD) instructions, comprising:

a single multiply-accumulate (MAC) unit for generating a first data result responsive to a first operand and a second data result responsive to a second operand, wherein said first and second operands are associated with a SIMD instruction;

means for storing the first data result;

~~means for generating a second data result responsive to a second operand;~~

means for generating an exception result responsive to the first and second data results;

means for forwarding the first data result and the second data result to a buffer when the exception result indicates that the first data result and the second data result are valid; and

means for communicating the exception to the buffer when the means for forwarding indicates that the first and second data results are invalid.

12. (Previously Amended.) The apparatus of claim 11, further comprising:

means for storing the first operand; and

means for storing the second operand.